DYLAN LEIFER-IVES

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OBJECTIVE

Highly driven Computer Engineering Student, focused on compilers and computer architecture. Eager to research into reconfigurable computing, aggressive optimizations, and general compiler-architecture interaction.

EDUCATION

Senior at California Polytechnic State University: San Luis Obispo. Graduates **June 2025** Bachelor's of Science in Computer Engineering (BSCE) **GPA: 3.4**

Relevant Coursework: Compiler Design, Computer Architecture, Systems Programming, Networks, UXIX, Embedded Systems, FPGA Design, Digital Design, Electronics, Electric Circuit Analysis & Lab I-III

Skills: C \ C++, python, Java, Logic Analyzer, Debugging, Version Control, Git, Microcontrollers, Verilog, VHDL, KiCad, Autodesk Eagle, LtSpice

PROFESSIONAL EXPERIENCE

Fluke Corporation

Employee: June 2024 - September 2024 | Everett, WA, USA

- Coordinated with cross functional teams to design and implement CI/CD automated firmware testing architecture and framework.
- Worked on Code Synthesis & Validation to translate in house testing programming language to Python.
- Worked on a source to source compiler to remove legacy in house language and code system.
- Used Agile methodologies to quickly iterate and integrate new development with both legacy and existing systems.

Ace Hardware

Employee: June 2023 - September 2023 | Fairfax, CA, USA

Glumac

Electrical Engineering Intern: June 2022 - September 2022 | San Francisco, CA, USA

RESEARCH

Dynamic CGRA Accelerator | FPGA, LLVM, AI/ML **September 2024 - Current**

In progress research into dynamically acceleration of processors by mapping instructions spatially.

- Designed and implemented a Coarse Grained Reconfigurable Array (CGRA) for dynamic acceleration of instructions.
- Implemented Out-of-Order execution pipelined processor, holding to the RISCV32i standard
- Developing LLVM-based compiler passes based around to optimize transformations and data mappings for CGRA fabrics.
- Using polyhedral and affine analysis for optimizing dependencies for the inherently dataflow optimized CGRA architecture.
- Focused on improving computational efficiency, reducing power consumption, and enhancing control dependencies in dynamic acceleration.

PROJECTS

Minilang Compiler | Zig, C, minilang **March 2024 - June 2024**

https://github.com/probably-neb/minipp

- An optimizing compiler written completely from scratch in Zig. Supports armV8 and LLVM as backends.
- Written using Agile & Test Driven Development methodologies. With SSA and stack transformations.
- Developed custom IR to support easy & modular implementation of backends. With per backend verification steps.

Arduino ML accelerator | SystemVerilog, IC design, FPGA **February 2023 - March 2023**

A test project to work on application of Computer Architecure to AI.

- Developed using Xilinx tools, embedded FGPA ML accelerator for an Arduino Mega over SPI.
- Implemented Automated Hardware Synthesis from a pretrained model in Python.
- Reduced running time for letter classification 30% when compared with MCU only solution.

RiskBoy | SystemVerilog, Verilog, RISC-V **September 2022 - January 2023**

A project to implement a full RISC-V cpu and custom GPU to run games.

- Implemented custom 5 stage pipeline RISCV32i processor. 64KB RAM, with a 400MHz clock.
- Implemented custom NES inspired GPU, supporting 640x480 at 60fps, with 256 colors in 16 swatches.
- Integrated into a handheld unit to allow for the running of games, like a gameboy.

Scroll Scribbler | C/C++, Zephyr/FreeRTOS **June 2020 - December 2023**

A 2D CNC machine that writes on scrolls, as a replacement for a printer

- Worked with a cross functional team to design and fabricate chassis and system.
- Writes a full 8.5”x11” page of text in 10 minutes.
- Uses SPI & UART, as well as custom communication protocol for increased image processing throughput.
- Small scale test automation & Firmware verification & validation.

8086 Laptop | C, x86ASM, UNIX **September 2023 - Present**

A Laptop based around the 8086 chip from the 70’s

- Designed and fabricated custom PCB board layout and design.
- Custom event based OS written in C. Utilizing TDD for shift left testing.

Interests: Computer Architecture, Embedded Systems, Verilog, C, C++, Figure Drawing, Olympic Lifting, Hacking old technology, Linguistics, Systems Programming